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A semi-analytical small signal parameter extraction method for millimeter HEMT

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Abstract: A semi-analytical small signal parameter extraction method for high electron-mobility transistor(HEMT) under different bias conditions is presented. Based on test structure to determine the pad capacitance and parasitic inductances, the semi-analysis method is used to extract parasitic resistances and to improve the precision of the parasitic resistance in the small signal model. The agreement between the measured S-parameters and simulated ones is excellent over the frequency range up to 40 GHz under multibias condition.

Key words: high electron-mobility transistor; parasitic resistances; multibias condition; semi-analysis method; small signal model

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一种基于半分析法的HEMT小信号参数的提取方法

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摘要：提出了一种基于半分析法的高速电子迁移率半导体晶体管小信号模型的提取方法.此方法是用测试结构的方法来提取焊盘电容和寄生电感，半分析法来提取寄生电阻，提高了寄生电阻的提取精度.在频率高达40 GHz的范围内，多偏置情况下模拟的S参数和测试的S参数曲线吻合良好，证明这种方法是正确的.

关 键 词：高速电子迁移率半导体晶体管;寄生电阻;多偏置情况;半分析法;小信号模型

中图分类号：TN386.6 **文献标识码**：A

Introduction

The high electron-mobility transistors are widely used in application including microwave sources and power amplifiers in microwave systems, which are readily integrated with passive elements to amplifiers for insertion into wireless communication infrastructure. As the small signal equivalent circuit models are frequently used in the design of linear millimeter-wave circuits, it is also a basis for large signal models[1].

Many procedure to extract the small signal equivalent circuit are based on optimization methods, which aims to calculate the value of parameters under active bias condition by fitting calculated S-parameters to measured ones. An important shortcoming of these techniques is that the element values would converge to nonphysical values due to the multiple local solutions of the optimized objective function. Another method is based on direct extraction which typically used cold-FET S-parameter measurement. Direct extraction techniques are faster than optimization-based ones, but they often require a subsequent optimization step to improve the fitting in active bias conditions.

In order to overcome these difficulties, a semi-analytical small signal parameter extraction method under different bias conditions is presented for the determina-

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tion of the parasitic resistances for HEMT. In contrast with previous publication, this method has the advantages as follows.

Normally only S parameters of the device are available, it is difficult to extract all the extrinsic elements according to the direct extraction. The semi-analysis method is very useful, the intrinsic elements determined by a described functions of the extrinsic elements. Assuming that the equivalent circuit composed of lumped elements is valid over the whole frequency range of the measurements, the extrinsic elements are iteratively determined using the variance of the intrinsic elements as an optimization criterion. Since the procedure would check out the value of parameters whether it is physical value, the parasitic resistance and other parameters would be valid and precise[2].

The extraction procedure has been successfully verified with measured S-parameter measurement data on HEMT up to 40 GHz In this paper. Section II explains the proposed extraction method of small signal equivalent circuit. The experiments and results are reported in Section III. Finally, Section IV discusses the conclusions.

1 Extraction procedure

Figure 1 shows the conventional small signal equivalent circuit model for HEMT which can be divided into two parts:

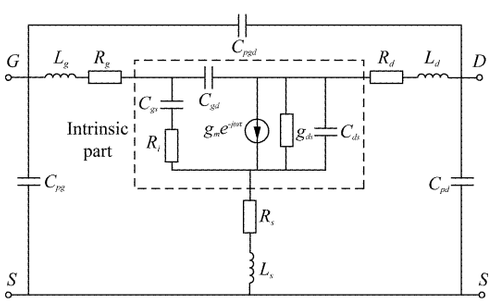

Fig. 1　Small-Signal Equivalent Circuit of HEMT
图 1　HEMT 小信号等效电路模型

(1) the intrinsic elements which consist of g_m, g_{ds}, C_{gs}, C_{ds}, C_{gd}, R_i, τ

(2) the extrinsic elements which consist of C_{pg}, C_{pd}, C_{pgd}, L_g, L_d, L_s, R_g, R_d, R_s

where L_g, L_d and L_s represent the inductances of the gate, drain and source feedlines, respectively, and C_{pg}, $C_{pd}$and C_{pgd}represent the pad capacitances. $R_s$and R_d are the source and drain resistances, and R_g is the distributed gate resistance. C_{gs}, C_{gd} and C_{ds} are the gate-to-source, gate-to-drain and drain-to-source intrinsic device capacitances, respectively. R_i is the channel resistance. g_m is the transconductance, $g_{ds}$is the drain conductance and $\tau$is the time delay associated with transconductance.[3]

The procedure can be summarized as follows.

1.1 Pad Capacitances

The pad capacitances are determined by measuring an open structure which consisted of only pads without the transistor. Measurements of the open structure are modeled as a pi network includingC_{pg}, $C_{pd}$and C_{pgd}[4][5]. Figure 2 shows the equivalent circuit model of open test structure. C_{pg}, $C_{pd}$and C_{pgd} can be directly obtained from the Y parameters of the open test structure.

$$C_{pg} = \frac{1}{\omega}\mathrm{Im}(Y_{11} + Y_{12}) \quad , \quad (1)$$

$$C_{pd} = \frac{1}{\omega}\mathrm{Im}(Y_{22} + Y_{12}) \quad , \quad (2)$$

$$C_{pgd} = -\frac{1}{\omega}\mathrm{Im}(Y_{12}) = -\frac{1}{\omega}\mathrm{Im}(Y_{21}) \ . \quad (3)$$

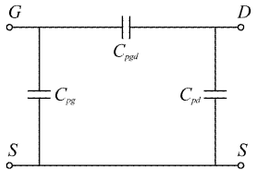

Fig. 2　Pad capacitances equivalent circuit of open test structure
图 2　开路测试结构的 PAD 电容等效电路

1.2 Parasitic inductances

The parasitic device-connection impedances can be determined by measuring a test pattern which consists of the pad, the device feeds and a short circuit in place of the transistor. The shorted test structure is modeled as a T-network of series resistances and inductors, as Figure 3 shows.[4][5]

The extrinsic inductances and feedline losses can be directly determined from Z parameters of the shorted test structure:

$$L_g = \frac{1}{\omega}(Z_{11} - Z_{12}) \quad , \quad (4)$$

$$L_d = \frac{1}{\omega}(Z_{22} - Z_{12}) \quad , \quad (5)$$

$$L_s = \frac{1}{\omega}(Z_{12}) = \frac{1}{\omega}(Z_{21}) \quad . \quad (6)$$

The feedline losses are very small and normally near to zero therefore can be neglected compared to the contact resistances.

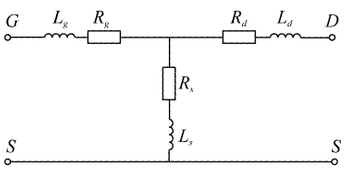

Fig. 3 Parasitic inductances equivalent circuit of short test structure

图3 短路测试结构的寄生电感等效电路

1.3 Parasitic resistances

Parasitic resistances are very difficult to compute from electrical measurements. The semi-analysis method to extract parasitic resistances is a hybrid method of optimization and analysis approach. The global semi-analysis extraction technique is based on the following steps.

1) Set up the initial values of the extrinsic elements which is based on cold-FET measurements.

2) Calculate the intrinsic parameters which can be expressed as the functions of the extrinsic elements as follows:

$$C_{gs} = f_1(R_g, R_s, R_d) \quad , \quad (7)$$

$$C_{gd} = f_2(R_g, R_s, R_d) \quad , \quad (8)$$

$$C_{ds} = f_3(R_g, R_s, R_d) \quad , \quad (9)$$

$$g_m = f_4(R_g, R_s, R_d) \quad , \quad (10)$$

$$g_{ds} = f_5(R_g, R_s, R_d) \quad , \quad (11)$$

$$R_i = f_6(R_g, R_s, R_d) \quad , \quad (12)$$

$$\tau = f_7(R_g, R_s, R_d) \quad . \quad (13)$$

For convenience, the function f can be expressed as:

$$f_k = f_k(\omega_i, Z_{ext})(k = 0, 1, 2) \quad , \quad (14)$$

where Z_{ext} represent the extrinsic elements, ω_i is the angular frequency.

It is well known that intrinsic elements can be determined directly after all the extrinsic elements are obtained[6]:

$$C_{gs} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega}\left[1 + \left(\frac{Re(Y_{11} + Y_{12})}{\mathrm{Im}(Y_{11} + Y_{12})}\right)^2\right] \quad , (15)$$

$$C_{ds} = \frac{\mathrm{Im}(Y_{22} + Y_{12})}{\omega} \quad , \quad (16)$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega} \quad , \quad (17)$$

$$R_i = \frac{Re(Y_{11} + Y_{12})}{\omega C_{gs}\mathrm{Im}(Y_{11} + Y_{12})} \quad , \quad (18)$$

$$g_m = |(Y_{21} - Y_{12})(1 + j\omega C_{gs}R_i)| \quad , (19)$$

$$g_{ds} = \mathrm{Re}(Y_{22} + Y_{12}) \quad , \quad (20)$$

$$\tau = -\frac{1}{\omega}\tan^{-1}\left\{\frac{\mathrm{Im}[(Y_{21} - Y_{12})(1 + j\omega C_{gs}R_i)]}{\mathrm{Re}[(Y_{21} - Y_{12})(1 + j\omega C_{gs}R_i)]}\right\} . (21)$$

3) Setup error criteria as follows,

$$\varepsilon_1^k(Z_{ext}) = \frac{1}{N-1}\sum_{i=0}^{N-1}\left|f_k(\omega_i, Z_{ext}) - \overline{\sum_{i=0}^{N-1} f_k(\omega_i, Z_{ext})}\right|^2 , (22)$$

$$\varepsilon_2(Z_{ext}) = \sum_{p=1}^{2}\sum_{q=1}^{2}\sum_{i=0}^{n-1}|S_{pq}^c(\omega i, Zext) - S_{pq}^m(\omega_i)|^2 \quad (p, q = 1, 2) \quad , \quad (23)$$

where $S_{pq}^c(\omega_i, Z_{ext})$ is the calculated S parameters, $S_{pq}^m(\omega_i)$ is the measured S parameters, $\varepsilon_1^k(Z_{ext})$ represent the frequency dependence of the intrinsic circuit elements, and $\varepsilon_2(Z_{ext})$ represent the fitness between measured S-parameters and simulated S parameters.

4) If error criteria are small enough, the iterative is over.

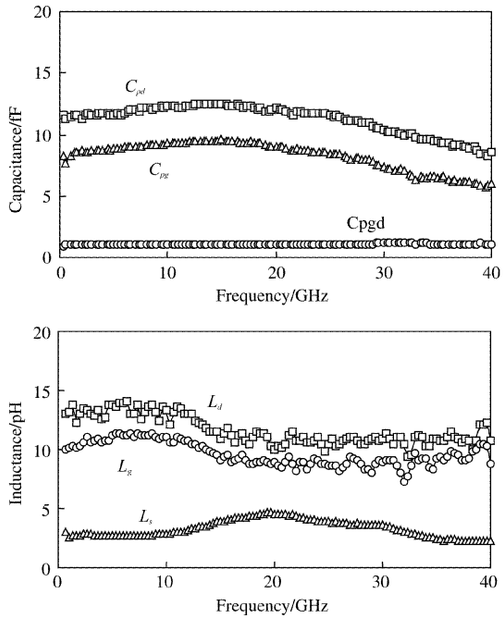

Fig. 4 Pad Capacitances and parasitic inductances extracted from test structure

图4 PAD电容和寄生电感的测试结构提取结果

2 Model identification

First, we determine the values of pad capacitances and parasitic inductances from the test structures which are shown in Fig. 4. The isolation between the pads is 35. 7 dB, which corresponds to a capacitance C_{pgd} of 1.06 fF.

Second, we extract the parasitic resistances using the semi-analysis method under single bias like V_{ds} = 2 V, V_{gs} = 0 V. The extracted results for the extrinsic elements are summarized in Table 1.

Table 1　Extrinsic parameters for HEMT
表 1　HEMT 的寄生元件值

C_{pg} = 8. 28fF	C_{pd} = 11.246fF	C_{pgd} = 1.06fF
L_g = 9. 62pH	L_d = 11.67pH	L_s = 3.32pH
R_g = 5. 41Ω	R_d = 1Ω	R_s = 4. 78Ω

In order to demonstrate the behavior of small signal model, we have extracted the equivalent circuits at 15 different bias points and the behavior of the intrinsic elements matches the theoretical expectations in Table 2[7].

The fit to the measured data is obtained by defining an error criterion between the measured and simulated data. The S parameter errors E_{ij} are defined as criteria:

$$E_{ij} = \left| \frac{S_{ij}^m - S_{ij}^s}{S_{ij}^m} \right| (i, j = 1, 2) \quad . \quad (24)$$

The average error percentages for HEMT under V_{ds} = 2V bias condition are summerized in Table 3. It is obviously that the error percentages are remained within an accuracy of 1%. The good agreement is obtained between measured and simulated S parameters as shown in Fig. 5.

Table 2　Equivalent circuit intrinsic elements under multibias condition
表 2　多偏置情况下的等效电路的本征元件

V_{ds}(V)	V_{gs}(V)	C_{gs}(fF)	C_{gd}(fF)	C_{ds}(fF)	g_m(mS)	g_{ds}(mS)	τ(ps)	R_i(Ω)
0.5	0.6	25.813	12.863	10.134	7.979	1.389	0.085	3.627
1.0	0.6	31.449	11.192	9.663	17.923	2.401	0.180	8.4
2.0	0.6	40.182	9.351	9.613	26.664	2.702	0.49	9
2.0	0.5	44.091	8.898	9.849	31.883	2.956	0.43	8.622
2.0	0.4	44.552	8.447	9.215	34.977	2.835	0.45	7.847
2.0	0.3	45.434	8.051	9.117	36.912	2.766	0.5	9.2
1.0	0.2	38.653	9.032	10.689	42.381	3.863	0.12	7.731
1.5	0.2	42.988	8.179	9.886	40.619	3.104	0.15	8.711
2.0	0.2	46.327	7.823	9.708	38.430	2.475	0.27	8.36
1.0	0.1	38.6	8.879	11.504	43.249	3.741	0.08	7.820
1.5	0.1	42.750	7.826	10.124	40.619	2.778	0.1	8.008
2.0	0.1	46.094	7.589	9.936	38.043	2.296	0.12	8.675
1.0	0	38.192	8.862	12.513	42.021	3.550	0.005	7.163
1.5	0	41.944	7.529	10.393	38.517	2.601	0.02	7.258
2.0	0	44.944	7.437	9.972	35.728	2.083	0.06	7.681

Table 3　Error percentage between simulated and measured S parameters, bias: V_{ds} = 2V
表 3　模拟和测试的 S 参数误差

V_{gs}(V)	S_{11}(%)	S_{12}(%)	S_{21}(%)	S_{22}(%)
0	0.131	0.399	0.526	0.148
0.1	0.101	0.411	0.407	0.124
0.2	0.115	0.396	0.504	0.074
0.3	0.145	0.283	0.971	0.164
0.4	0.17	0.245	0.572	0.138
0.5	0.157	0.296	0.751	0.131
0.6	0.159	0.192	0.713	0.131

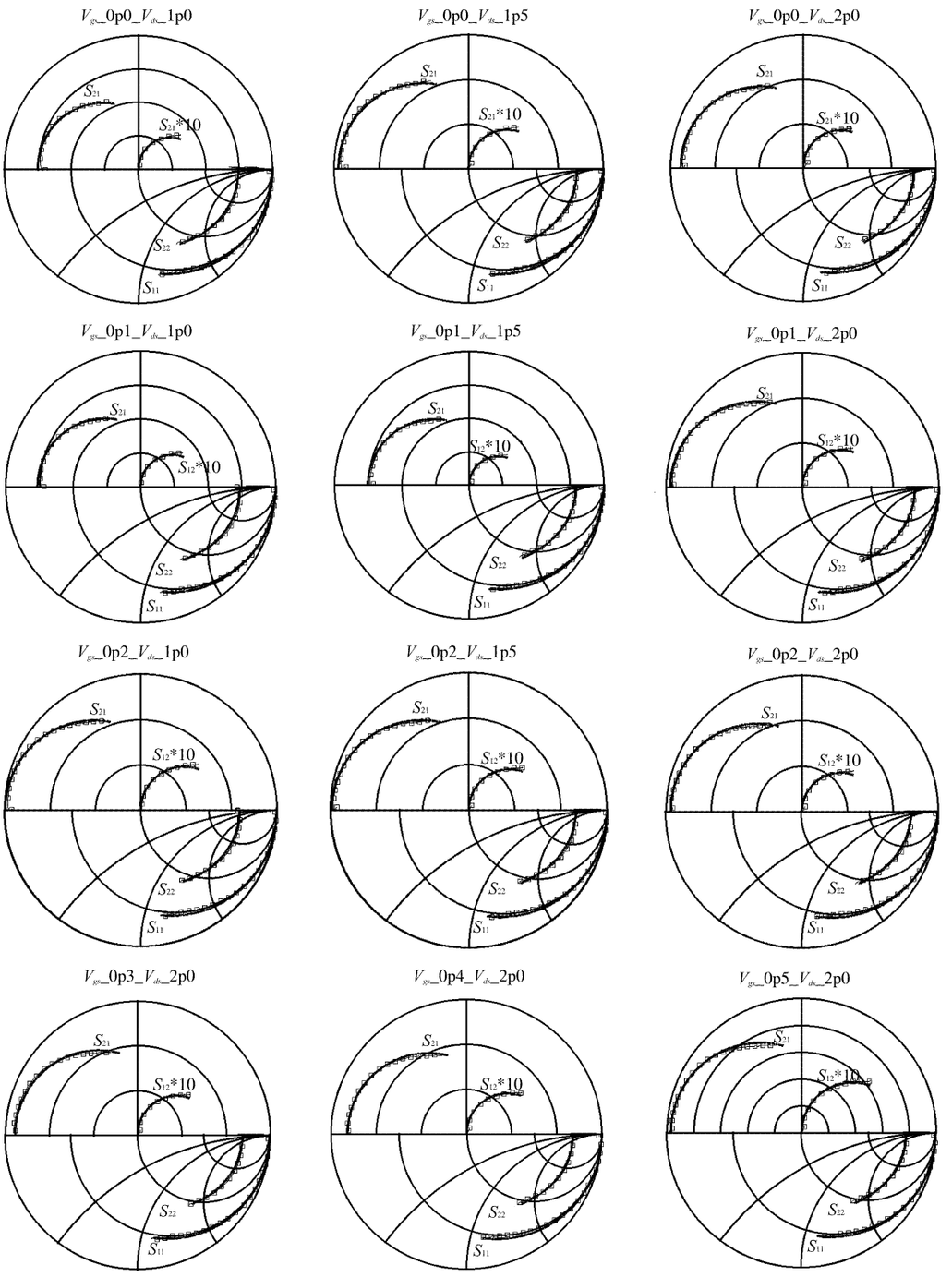

Fig. 5 Modeled and measured s-parameters for HEMT under different bias
图5 HEMT在多偏置情况下模拟和测试的 S 参数对比

3 Conclusion

An accurate extraction method for extrinsic parameters has been proposed. The semi-analysis method can provide an approach to estimate the values of parasitic resistances which are physical and precise. The accuracy of the extracted equivalent circuits has been verified though the good agreement between measured and

simulated S-parameters under all investigated bias conditions. In addition, the proposed method has been confirmed by the intrinsic elements, which agrees with the theoretical expectations.

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3 Conclusions

Principles of the continuous zoom system with large zoom range are introduced. A MWIR continuous zoom system with 320 × 240 staring FPA was designed, which can realize zoom range of 45. The system has high image quality and satisfies 100% cold shield efficiency. MWIR continuous zoom system with large zoom range has an enormous potential for many applications such as tracking and surveillance.

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